What is claimed is:

1. A semiconductor memory device comprising:

a semiconductor substrate;

a first interlayer insulating layer formed on the semiconductor substrate;

a plurality of first conductive layers spaced apart from each other on the first interlayer insulating layer;

a second interlayer insulating layer formed on the plurality of first conductive layers;

a plurality of second conductive layers spaced apart from each other on the second interlayer insulating layer; and

a plurality of connecting devices formed in the first and second interlayer insulating layers, the plurality of connecting devices for connecting the first and second conductive layers,

wherein the connecting devices each include at least one plug extending from the semiconductor substrate to the lower portion of the second insulating layer and a pad formed in the upper portion of the second insulating layer for connecting the at least one plug and one of the second conductive layers, and wherein the pad has an upper width such that the pad connected to one of the second conductive layers does not contacts another one of the second conductive layers to prevent a short circuit therebetween.

2. The semiconductor memory device of claim 1, wherein the height of the at least one plug is greater than twice the height of the pad.

3. The semiconductor memory device of claim 2, wherein the connecting devices further comprise a second plug for connecting one of the first conductive layers and the semiconductor substrate, and the height of the second plugs is 30 - 50% of the height of the at least one plug.

4. The semiconductor memory device of claim 3, wherein the height of the at least one pad is no greater than the height of the second plug.

5. The semiconductor memory device of claim 3, wherein the connecting devices further comprise NMOS transistors which control the electrical connection between the second plugs and the at least one plug.

6. The semiconductor memory device of claim 4, wherein the connecting devices further comprise NMOS transistors which control the electrical connection between the second plugs and the at least one plug.

7. A semiconductor memory device comprising:

a semiconductor substrate;

a first interlayer insulating layer;

a plurality of local bit lines spaced apart from each other and disposed on the first interlayer insulating layer;

a second interlayer insulating layer on the plurality of local bit lines;

a capacitor formed on the second interlayer insulating layer and electrically connected to the semiconductor substrate;

a plurality of global bit lines which are spaced apart from each other and are disposed on the second interlayer insulating layer; and

a plurality of connecting devices formed in the first and second interlayer insulating layers, and each connecting device electrically connecting the plurality of local bit lines and the plurality of global bit lines,

wherein each connecting device has a pad directly connected to one of global bit lines, first plugs connecting the semiconductor substrate to one of the local bit lines, a connector extending from one of the local bit lines and electrically connecting one of the local bit lines to the first plugs, and second plugs formed in the first and second interlayer insulating layers, connected to the pad, and connected to the first plugs via the semiconductor substrate, wherein the second plugs are wider toward the upper portion of the second interlayer insulating layer, the upper portion of the second plugs is not connected to the upper portion of an adjacent second plugs, the lower width of the pad is less than the upper width of the second plugs, and the pad has an upper width such that one of the global bit lines connected to the pad is not electrically connected to an adjacent global bit line via the pad.

8. The semiconductor memory device of claim 7, wherein the pitch of the global bit lines is equal to the pitch of the connector.

9. The semiconductor memory device of claim 8, wherein the height of the second plug is 2 - 4 times the height of the pad.

10. The semiconductor memory device of claim 7, wherein the pitch of the connector is twice the pitch of the global bit lines.

11. The semiconductor memory device of claim 10, wherein the height of the second plugs is four times the height of the pad.

12. The semiconductor memory device of claim 7, wherein the height of the first plugs is equal to or less than the height of the pad.

13. The semiconductor memory device of claim 7, wherein the connecting devices further comprise a circuit device which is formed on the semiconductor substrate and controls the electrical connection between the first and second plugs.

14. The semiconductor memory device of claim 13, wherein the circuit device is an NMOS transistor, and the first and second plugs are each connected to source and drain areas of the NMOS transistor.

15. The semiconductor memory device of claim 7, wherein the upper surface of the second plugs is positioned higher than the upper surface of the capacitor.

16. A method of manufacturing a semiconductor memory device, comprising:

forming a first interlayer insulating layer on a semiconductor substrate;

forming a plurality of first conductive layers spaced apart from each other and disposed on the first interlayer insulating layer;

forming a second interlayer insulating layer on the plurality of first conductive layers;

forming a plurality of second conductive layers spaced apart from each other and disposed on the second interlayer insulating layer; and

forming a plurality of connecting devices formed in the second interlayer insulating layer and connect the first conductive layers and the second conductive layers via the semiconductor substrate,

wherein the connecting devices each comprise at least one plug formed from the semiconductor substrate to the lower portion of the second interlayer insulating layers, a pad formed in the upper portion of the second interlayer insulating layer and electrically connecting the at least one plug and one of the second conductive layers, and a second plug connecting one of the first conductive layers and the semiconductor substrate, wherein the pad has an upper width such that one of the second conductive layers connected to the pad is not short-circuited to an adjacent second conductive layer via the pad.

17. The method of claim 16, wherein the height of the at least one plug is greater than twice the height of the pad.

18. The method of claim 16, wherein the height of the second plugs is 30 ~ 50% of the height of the at least one plug.

19. The method of claim 17, wherein the height of the pad is approximately equal to the height of the second plug.

20. A method of manufacturing a semiconductor memory device, comprising:

preparing a semiconductor substrate;

forming a connection control transistor on the semiconductor substrate;

forming a first interlayer insulating layer having first and second plugs each connected to source and drain areas of the connection control transistor on the surface of the semiconductor substrate on which the connection control transistor is formed;

forming a connector connected to the first plugs and a local bit line connected to the connector on the first interlayer insulating layer;

forming a second interlayer insulating layer having third plugs connected to the second plugs, the second interlayer insulating layer overlying the connector and the local bit line;

forming a third interlayer insulating layer having a pad therein on the second interlayer insulating layer, the pad connected to the third plug; and

forming a global bit line on the third interlayer insulating layer having the pad,

wherein an upper portion of the third plugs is not connected to the upper portion of an adjacent third plug, the lower width of the pad is less than the upper width of the third plug,

and the pad has an upper width such that the global bit line connected to the pad is not short-circuited to an adjacent global bit line via the pad.

21. The method of claim 20, wherein the pitch of the global bit line is equal to the pitch of the connector.

22. The method of claim 21, wherein the height of the third plugs is 2 - 4 times the height of the pad.

23. The method of claim 20, wherein the pitch of the connector is about twice the pitch of the global bit line.

24. The method of claim 23, wherein the height of the third plug is greater than four times the height of the pad.

25. The method of claim 20, wherein the height of the second plugs is no greater than the height of the pad.

26. The method of claim 20, wherein the pad is formed using a damascene process.

27. The method of claim 20, wherein forming the connection control transistor comprises forming a cell transistor in a cell array area of the semiconductor substrate.

28. The method of claim 27, further comprising forming a capacitor insulated from the local bit line and connected to source and drain areas of the cell transistor between the steps of forming the local bit line and the third plugs.

29. The method of claim 28, wherein the upper surface of the third plugs is positioned higher than the upper surface of the capacitor.

30. A semiconductor memory device comprising:

a semiconductor substrate;

a first interlayer insulating layer formed on the semiconductor substrate, the first interlayer insulating layer having a plug electrically connected to the semiconductor substrate;

a second interlayer insulating layer formed on the first interlayer insulating layer; and

a plurality of patterned conductive layers spaced apart from each other on the second interlayer insulating layer, and

wherein the second interlayer insulating layer has a connection pad formed therein, the pad disposed between the plug and one of the patterned conductive layers to electrically connect the plug and the patterned conductive layers, and

wherein the pad has an upper width such that the pad connected to one of the conductive layers does not contact another one of the patterned conductive layers to prevent an electrical short between the patterned conductive layers.